ABSTRACT OF THE DISCLOSURE

An overcurrent protection circuit (6) outputs an overcurrent protection signal (S6) based on a sense voltage (V_{sense}). A masking circuit (5) is configured so as to allow a masking signal (S5) to be kept set to "L" even when an input signal (IN) rises to "H" (an IGBT (1) is turned on) and an NPN bipolar transistor (23) is turned off, and allow the masking signal (S5) to be changed only after a capacitor (C12) is charged up and a voltage (V9) exceeds a reference voltage (VR). An AND gate (25) receives the masking signal (S5) at one of input terminals thereof and the overcurrent protection signal (S6) at the other of the input terminals thereof, and provides an output which is then output as an interruption control signal (SC_OUT) from a sense output terminal (P2) and is finally supplied to a gate terminal (P3) of the IGBT (1).